Audio applications efficiently apply sigma delta modulation techniques owing to their advantages in terms of aliasing, signal distortion and compatibility with modern microelectronic fabrication processes. In a sigma delta analog-to-digital converter, both the modulator and the digital decimation filter form the fundamental building blocks, defining the converter’s performance. Many degrees of freedom exist to design a digital decimation filter on silicon, such as the number of cascaded filter stages, chosen filter topologies, and selection of hardware-efficient filter architectures (e.g. polyphase filters).

This master thesis is about analyzing and implementing a hardware-efficient digital decimation filter for an existing audio sigma delta modulator. The filter should offer an optimal compromise in terms of current consumption, chip area, performance, and testability. The work will include literature studies, theoretical studies of different filter topologies, high-level simulations in Matlab, and the implementation of a decimation filter prototype.

Diploma Thesis overview:
• Character: 40% Digital filter theory, 30% Simulations, 30% VHDL/Implementation
• Prerequisites: Interest in digital signal processing, experience in MATLAB and VHDL is an advantage, willing to perform master thesis in industry.
• Timeframe: 6 months (diploma thesis)

This project offers the candidate an excellent opportunity to get involved in the design process of integrated digital circuits, and to gain experience on how to apply advanced mathematical signal processing concepts in a practical real world audio application.

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Contacts for additional information about this project:
austriamicrosystems AG
Dipl.-Ing. Matthias Steiner
Senior Design Engineer
Schloss Premstätten, A 8141 Unterpremstätten
phone: +43 3136 500 5967
e-mail: matthias.steiner@austriamicrosystems.com

Institut für Elektronik
Dipl.-Ing. Dr.techn. Mario Auer
Wissenschaftlicher Mitarbeiter
Inffeldgasse 12/I, A 8010 Graz
phone: +43 316 873 7538
e-mail: mario.auer@tugraz.at